



Minutes of P-1 Committee on Resistive Devices

Tuesday, 20 April, 2004

Hilton Tampa Westshore

Tampa, FL

P-1 Committee's Scope: All types of resistive components regardless of technology. Includes composition, film, wirewound, thermistors, attenuators, networks, and chip resistors and excluding Integrated Passive Devices.

Attendees:

NAME	COMPANY
Joe Biernacki	SEI-Electronics, Inc.
Jim Canner	Murata Electronics
Terry D. Charles	Panasonic
Ted Coler	Vishay
Michael Griffith	KOA
Nick Holmberg	Intel Corporation
Steve Olster	Mini-Systems Inc
Brian Piscitelli	KOA Speer Electronics
Dave Ritchey	Yageo
Liwu Wang	AEM

1.0 Introductions

Chairman **Brian Piscitelli** called the meeting to order at **4:05 p.m.**. A quorum was present.

2.0 Committee Organizations and Procedures

2.1 Membership

Attendance taken, and it was determined that a quorum was present.

62015:5/04

An attendance sheet was circulated and self-introductions were made.

<u>Member Organizations Present</u>	<u>Present at this meeting</u>	<u>Present at previous meeting?</u>	<u>Present at meeting prior to previous?</u>
AEM	Y*	n/a	n/a
Intel Corporation	Y*	n/a	n/a
KOA Speer Electronics	Y	Y	Y
Mini-Systems Inc	Y	N	Y
Murata Electronics	Y*	n/a	n/a
Panasonic	Y	Y	Y
SEI-Electronics, Inc.	Y	Y	N
Vishay	Y	Y	Y
Yageo	Y	Y	Y

*Activated as member of committee

<u>Member Organizations Absent</u>	<u>Present at This Meeting?</u>	<u>Present at previous meeting?</u>	<u>Present at meeting prior to previous?</u>
CTS*	N	N	N
Visteon	N	N	Y

*Not used in determination of quorum due to record of non-attendance

<u>Other Organizations Present</u>
EIA/ECA

2.2 Approval of Agenda

The Committee unanimously accepted the Agenda as presented.

2.3 Approval of October 2003 Meeting Minutes

The Committee unanimously accepted the Minutes of the last meeting as with changes to voting members

2.4 Correspondence

Received e-mail from P-4 to review component dimensions and conform to PDP-100 requirements.

2.5 Review of Committee's Scope – “ All types of resistive components regardless of technology. Includes composition, film, wirewound, thermistors, attenuators, networks, and chip resistors and exclude Integrated Passive Devices.”

Scope is fine as written.

2.6 DSCC Report

DSCC was not present at this meeting – no report was provided.

3.0 Old Business

3.1 Follow up of the proposed changes for ESD tests in EIA/IS-703 – Brian Piscitelli and Ed Mikoski

3.1.1 Requested PN number and sent electronic version to Ed for updating of the 0.25% to “Per Users Spec.”

A form was submitted for a new P/N and the electronic version was submitted to Ed Mikoski for publication.

Action item: resend PINS form and document, which has already been approved. The committee has approved to move this document to Ed Mikoski for SP Balloting

3.2 Review Comments from the ballots of both EIA-576-A, EIA-575-A

EIA-575-A(SP5052)

Modifications were requested by some members from the original voting ballot. These members voted yes but with comments to be considered by the group.

IBM –

- 1) would like to see 2 additional test methods included in the spec.
 - a. load humidity with full voltage applied (discussed by the committee members but rejected by the committee)
 - b. add reference to JIS-C-5202 for board bend test (discussed by the committee members but rejected by the committee)

MINI-SYSTEMS-

- 1) would like to see table 4 of standard Resistance values indicate tolerance from 5% to 5%/2% and 1% to 1%/0.5% (moved to accept)
- 2) add wording to 3.8 change from “No part of the clip jaw shall make contact with either termination nor have sufficient tension to mechanically damage the resistor element’s protective coating.” To “No part of the clip jaw or **tweezers** shall make contact with either termination nor have sufficient tension to mechanically damage the resistor element’s protective coating.”
- 3) Page 8 3.10 recommend adding wording to method 106 of Mil-STD-202 “step 7b is not applicable” (moved to accept)
- 4) Paragraph 3.12.1 (solderability) request to change to J-STD-002 instead of J-STD-004 (approved)

- 5) Requested test groups should be 4 instead of 3 groups (not approved by committee)
- 6) Page 9 3.12.2 (remove item "D") – already covered by 260°C temperature testing.(approved)

SP5052 was voted at the April meeting. Tally as follows:

Murata – Abstain
Panasonic – 30 day extension to vote
Intel – Abstain
Vishay – Yes
Yageo –Yes
Compaq –no response
KOA – Yes
ROHM – no response
IBM – Yes
AEM – Yes
Mini-Systems – Yes
CTS – no response
SEI - Yes

Upon receiving Panasonic response SP5052 will move to next step of voting process.

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Compaq –no response
KOA – Yes

ROHM – no response
IBM – Yes
AEM – Yes
Mini-Systems – Yes
CTS – no response
SEI - Yes

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3.3 Review and addition of Resistor outlines to the newly formatted/web-based PDP-100

A review of all mechanical drawings was performed by the members.

SOGC-1102 (not for new format)
SOGC-1405 (not for new format)
SOGC-2308 (not for new format)
SOGC-6320 (not for new format)
SOMM-2012 (change for new format) – Yageo (Dave Ritchey)
SOMM-3216 (change for new format) – Yageo (Dave Ritchey)
SOMM-3514 (change for new format) – Vishay (Ted Coler)
SOMM-5922 (change for new format) – Vishay (Ted Coler)
SOPC-1106 (change for new format) – Panasonic (Terry)
SOPC-2107 (change for new format) – Panasonic (Terry)
SOPC-6235 (change for new format) – KOA (Mike G)
SOPC-9941 (change for new format)- KOA (Mike G)

The following drawings need to be reviewed and to meet new PDP-100 standard formatting.
SOCM-1005, 1608 (SEI -), 2012, 3216 (Mini-systems – Stephan Olson), 3225, 5025, 6332 (KOA Brian P.)
Require drawings for SOCM-0603 (SEI), 3246 (Vishay Ted Coler) to be created to new PDP-100 requirements to cover all chip resistors.

Brian Piscitelli to e-mail PDP-100 part numbering scheme to all those performing the changes to the drawings.

3.4 Review proposed changes to EIA-886 and EIA-887 – Ted Coler

Motion to move EIA-886 & 887 to submit p/n for letter balloting.

3.5 Start the process of generating a thin film on ceramic resistor array spec.

Motion to submit a PINS for thin film on ceramic array for letter balloting

3.6 Review open P-1 projects

No new open projects were requested to be started.

3.7 Pb-free Updates

JEITA ETR-7021 – guidelines for marking of “Pb” free components. This requirement was discussed. Intel has a possible requirement to mark all “Pb” free parts with the marking per ETR-7021. Nicholas (Intel) is going to review this with his people and report back to the committee in October 2004.

3.8 Other

4.0 New Business

No new business was discussed.

4.1 Other

5.0 Next Meeting

The next meeting is scheduled to be held during the ECA Fall Engineering Summit October 4-7 Holiday Inn On-the-Bay, San Diego, CA.

6.0 Adjournment

Meeting adjourned at **6:00 p.m.**

This meeting was conducted in accordance with the EIA Legal Guidelines and the Manual of Organization and Procedures.

Brian Piscitelli
Chairman

Mike Griffith
Secretary